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Department of Electrical Engineering

LESSON PLAN

SESSION:2026-2027

Discipline: Electrical Engg.	**Semester: 5th**	**Name of the Teaching Faculty : NIBEDITA HO**
Subject:DIGITAL ELECTRONICS AND MICROPROCESSOR	**No. of Days/per week class allotted:3**	**Semester from date: 01.07.2026 To Date: 05.11.2026** **No. of Weeks:15**
Week	**Class Day**	**Theory**
1st	1st	**DigitalFundamentals** Number Systems – Decimal, Binary
	2nd	Octal, Hexadecimal
	3rd	1's and 2's complements, Codes – Binary, BCD
2nd	1st	Excess 3, Gray, Alphanumeric codes
	2nd	Booleantheorems,Logicgatesandtruthtables
	3rd	Universalgates
3rd	1st	Sumofproducts andproductofsums,MintermsandMaxterms
	2nd	KarnaughmapMinimizationand QuineMcCluskey method of minimization.
	3rd	**Combinational&SynchronousSequentialCircuits** DesignofHalf Adder
4th	1st	DesignofFullAdder
	2nd	DesignofHalfSubtractor

	3rd	DesignofFullSubtractor
5th	1st	BinaryParallelAdder
	2nd	Multiplexer, Demultiplexers
	3rd	Decoders, andPriorityEncoder
6th	1st	Flip flops – SR,JK
	2nd	Flip flops -T, D
	3rd	Design of clocked sequential circuits- Design of Counters
7th	1st	Shift registers, Universal Shift Register.
	2nd	**AsynchronousSequentialCircuits** Stable and Unstable states
	3rd	output specifications, cycles and races
8th	1st	state reduction, race free assignments
	2nd	Hazards, Essential Hazards,
	3rd	Pulse mode sequential circuits, Design of Hazard free circuits.
9th	1st	Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM
	2nd	RAM – Static and dynamic RAM
	3rd	Programmable Logic Devices- Programmable Logic Array (PLA)
10th	1st	Programmable ArrayLogic(PAL)
	2nd	Field ProgrammableGate Arrays (FPGA)
	3rd	**8085Processor** HardwareArchitecture
11th	1st	Pindiagram
	2nd	FunctionalBuildingBlocksofProcessor

	3rd	Memory organization – I/O ports and data transfer concepts
12th	1st	Timing Diagram – Interrupts.
	2nd	Timing Diagram – Interrupts.
	3rd	**ProgrammingProcessor** Instruction – format
13th	1st	Addressing modes
	2nd	Assembly language format – Data transfer
	3rd	Assembly language format – data manipulation & control instructions
14th	1st	Programming: Loop structure with counting & Indexing
	2nd	Programming: Loop structure with counting & Indexing
	3rd	Look up table
15th	1st	Subroutine instructions, stack
	2nd	8255 architecture
	3rd	operating modes

Course outcomes: After completion of the course, the students will be able to

CO1:Design Logic circuits using basic concepts of Boolean algebra.
CO2:Design any Logic circuit using basic concepts of PLDs.
CO3: Develop applications using 8085 Microprocessor.
CO4:Develop 8085 interface using programmable I/O device.

29.05.26

Signature of the faculty